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Design rule of swift Control Prototyping Systems for Power Electronics and Electrical Drives

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***Abstract*—It has 4 speedy organize prototyping organization planned intended for manage of supremacy electronics in addition to electrical impel. 3 dissimilar, except steadily enhanced quick managescheme improved inside academe plus a profitable SCALEXIO scheme as of production be initiate plus additional evaluate. The chief problem of a profitable quick manage prototyping scheme be charge. Its surroundings show the way toward the design toward employ thechief computer of a typical PC toward perform the genuine instance job. intend strategy resolve exist agreed through plus sw explanation of the quick organize prototyping scheme. The trial consequences get via scheme be as well agreedtoward here its recital.**

***Index Terms*—quick organize prototyping, Pentium structure, FPGA, dSPACE, PE, Electrical drives.**

preface

RCP be a extremely competent way toward increase, reduce, plus examination original organize policy within actual situation fast lacking handbook encoding. A RCP scheme support resting on principles PCs by RTAI Linux as RTOS be designed inside Wuppertal academia [1]. while the concurrent addition in support of Linux be accessible, and altered toward Linux.

A Field Programmable Gate Array support instantaneous run scheme function below RTAI Linux be planned inside [5]. The CPU unit be considerably enhanced description of the Pentium M method. The matter charge of the Pentium 4 or Pentium M scheme assortment as of 1500 EUR to 2000 EUR.

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by the expansion of original topologies plus original run plan inside PE plus electrical make, a influential concurrent manage scheme be needed. in addition, the enter intended for the subsequently vital pace towards an power capable globe deceit inside the original equipment, such since extensive posse hole semiconductors which permit intended for superior supremacy competence, lesser extent, lesser in general charge - otherwise every of the jointly. The augment of control occurrence designed for a motor by SiC support supremacy semiconductor too require extra influential concurrent manage scheme. intended for conquer the subject, a UltraZohm scheme support on top of a ZU9EG by elevated presentation ability be planned [6]. ZU9EG machine inside line an FPGA by numerous ARM Cortex^{TM} , manufacture the statement extremely quick vigorous plus simple in the direction of exercise.

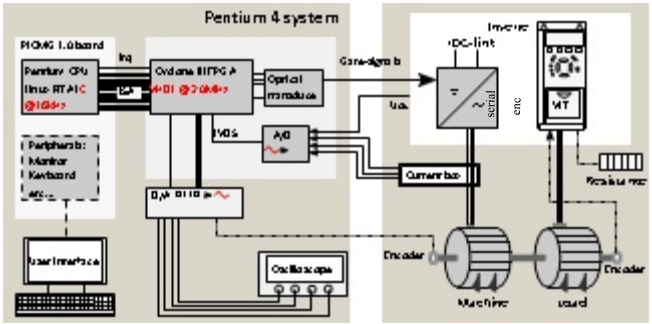
by observe toward the profitable goods, a SCALEXIO scheme as of dSPACE be fit used for RCP request [7]. The HW contain the cover plus the concurrent HW, such since dispensation component plus I/O HW. intended for the contrast by the over state scheme, a easy explanation of SCALEXIO scheme determination exist too incorporated.

HW EXPLANATION

Three dissimilar RCP scheme improved inside university plus 1 viable RCP scheme as of dSPACE inside manufacturing determination exist obtainable. inside arrange in the direction of there it is additional evidently, contrast amongst the RCP scheme plus the chief processors be primary specified.

A. Pentium M structure

RCP scheme support on top of a Pentium M scheme intended for manage of PE plus electrical make. It be designed inside the EM plus make lab at Wuppertal campus, Germany.



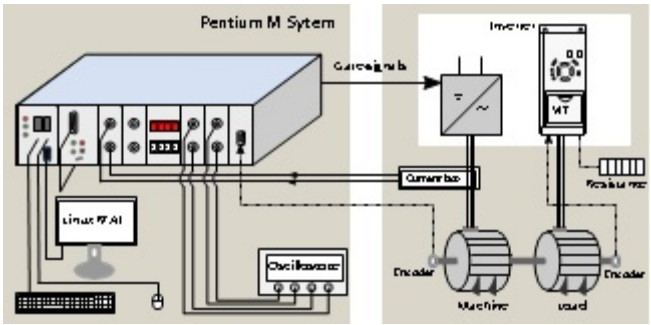


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Fig. 1: RCP scheme support on top of Pentium M scheme and it mostly having 19-inch Rack Chassis prepared by dissimilar useful panel otherwise cards.

- PC/104 CPU module measurement is a normal distinct via PC/104 group plus fits straight put in taken with the 19-inch rack.

PWM plank holds PWM indication making, manage PWM departed instance designed for IGBT, plus disrupt creation. Three PWM indication making ways: sin, SVM, plus straight modes.

A/D C tag employ A/DC MAX120, have 2 direct plus by means of a ruling of 12 bit & change instance 1.6 μs.

- D/AC license employ D/AC AD667, have 2 strait plus by a declaration of 12 bit & situation occasion 3 μs.
- Encoder plank encoder kind 05.2400 as of Kübler by a motion of 1024 pulsate for each insurrection be employ.
- HEX license by a 16 bit hexadecimal exhibit plus exercise toward modify changeable standards within the algorithm as the system be implemented.

RCP scheme exclusive of by DSP preserve without difficulty execute FOC technique of initiation mechanism by 12 kHz manage freq. The trial consequences of PTC technique executeon a stage motor experiment worktable resolve live agreed inside part.

devise principle 1: rate deliberation

B. Pentium 4 scheme

RCP classification support resting on a Pentium 4 scheme designed for organizes of PE plus electrical make. It be designed within the manage of EDS plus PE on technological campus of Munich.

The Pentium 4 scheme be a appreciably enhanced description of the Pentium M structure. The diagram of the Pentium 4 scheme be represent within the missing fraction of Fig, which largely having

- 19-inch Rack Chassis, PICMG 1.0 key panel, FPGA panel, which the in turn interactions amid additional panels be feasible, CPLD panel, D/A plus encoder panel, Current capacity panel, HEX license.

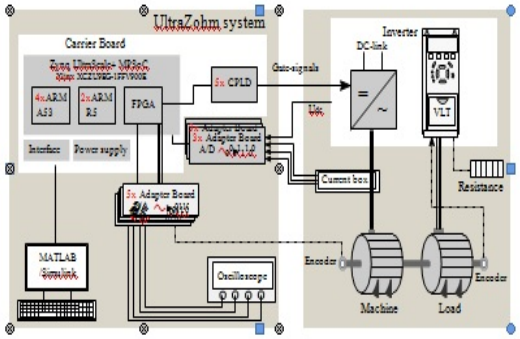

Fig. 3: RCP system based on a UltraZohm system

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The fundamental process of the superior scheme be the identical as designed for the Pentium M scheme employ intended for the two-stage motor experiment worktable. The trial consequences of the PTC technique execute resting on a three-stage motor experiment worktable determination exist in Part.

intend principle 2: scheme modernize

C. UltraZohm structure

RCP scheme support on top of a UltraZohm scheme proposed intended for a extensive choice of PE support scheme. It be together designed via analyzers. The scheme be particularly helpful used for calculation ally concentrated algorithms plus request by elevated difficulty lying on the no. of requisite capacity plus opening indication. The representation of the UltraZohm scheme be represent inside the gone element of Fig., which primarily having of:

- 19-inch Rack frame: It is prepared by dissimilar useful panel before cards transporter panel, which is the stamina of the scheme plus have the computation component, characteristic line plus power give.
- Analog Adapter panel: Two category of A/D Adapter panel are calculated designed for dissimilar functions. single employ A/D C MAX 11331, an additional employ A/DC ADS5272.
- Digital Adapter panel: 5 digital clamp socket inside transporter panel which offer within whole 136 digital contribution otherwise productivity. The D/A adapter panel that appreciate 16 visual source plus three visual beneficiary toward line a three stage motor by an extra indication intended for the DC-link dicer. RCP scheme be appropriate designed for execution of compound manage algorithms otherwise compound motor topology by elevated no. of I/Os . intended for additional permanence, the structure be immobile inside the procedure of expansion. The trial consequences of the shortest MPC technique execute on top of a two-stage motor experiment worktable determination exist specified inside Part IV.

intend principle 3: opposite promising test

A. SCALEXIO structure

SCALEXIO structure appropriate in favor of fast manages prototyping purpose. SCALEXIO structure to have of SCALEXIO LabBox by a DS6001 Processorpanel plus I/O panel fix.

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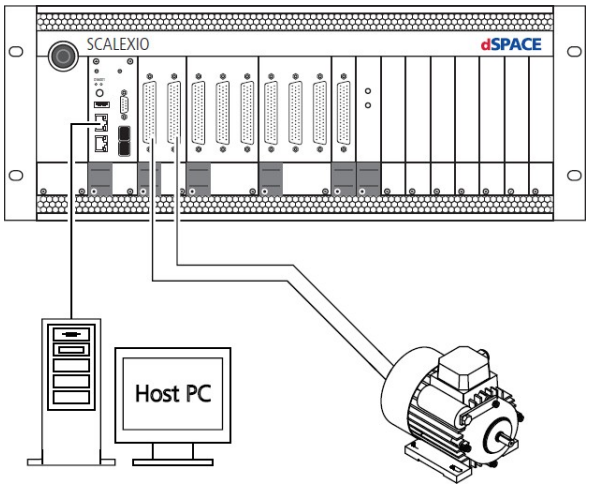

Fig. 4: RCP scheme support resting on a SCALEXIO scheme what time a SCALEXIO scheme be employ designed for fast manage prototyping, it manage a illicit scheme in its place of an ECU.The SCALEXIO scheme have to be capable toward:

- obtain the indication as of sensors
- make the indication intended for the actuators
- obtain bus indication which be throw via extra ECUs plus throw bus indication toward extra ECUs.

a number of fundamental panel be exercise toward collect a RCP organization designed for PE in addition to electrical make functions.

19-inch Rack structure: It be able to exist prepared by dissimilar useful panel.

- DS6001 Processor panel: It give elevated calculation supremacy plus tough concurrent presentation, by least jitter plus latency.
- FPGA support panel: An FPGA support panel within a SCALEXIO scheme have of an FPGA support panel plus positive in the direction of five connected I/O component plus associated using exact band wire. Three dissimilar kind FPGA stand panel be obtainable.
- DS6221 A/D panel: It give 16 discrepancy participation plus 8 added activate effort by a declaration of 16 bit plus exchange instance 250 ns.
- DS6241 D/D panel: It offer 20 direct by analog electrical energy productivity in addition to 4 extra activate effort plus by a declaration of 12 bit as well as scenery time 5 μs.

The manage algorithms be executed inside a immediate request which sprint on top of the processor panel. The concurrent request be shaped on top of the multitude PC plus downloaded toward the SCALEXIO scheme using Ethernet. A congregation PC be linked toward the SCALEXIO structure using Ethernet. SW tackle organization resting on a congregation PC be exercise toward effort by the SCALEXIO scheme.

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propose principle 4: presentation deliberation

SW explanation

intended for a RCP scheme, it is essential toward decide a correct OS scheme, which permit elevated competence, concurrent submission hold, short suspend latency, customer responsive line plus short charge as well, plan arrangement intended for dissimilar scheme too require toward be correct intended

A. instantaneous OS

since explain inside Table I, Linux be chosen since an OS intended for Pentium M plus Pentium 4 scheme. as typical Linux be not a tough immediate OS, the RTAI intended for Linux explain inside [8] be a practical plus efficient explanation intended for addition solid concurrent potential.

on behalf of the UltraZohm structure, on the minute it exercise a liberated R- TOS organization plus exposed metal designed for the manage. The major plus be by the FPGA since an "accelerator" designed for purpose to be parallelizable. The extra original end be concluding the organize circle straight resting on the FPGA lacking available during the CPU, which create it a group earlier.

by view toward SCALEXIO scheme, a profitable QNX RTOS be selected. The QNX Neutrino RTOS be a filled mark plus vigorous OS calculated toward allow then creation yield intended for automotive, remedial plus manufacturing scheme. It supports intended for the newest ARMv8 plus x86-64 processors. Of path, it too carry on toward carry 32-bit ARMv7 plus x86 processors.

break off Latency be a vital criteria intended for RTOS, so, the break off latency of normal Windows, Linux, plus Linux by dissimilar kernel be review within Table III.

TABLE III: Comparison between RTOSs [3].

Operating System	Application	Maximal Latency time
Standard Windows	No Real-Time	1 ms - 255 ms
Standard Linux	Soft Real-Time	up to 100 ms
Micro-Kernel	Hard Real-Time	1 - 10 μs
RTAI Linux	-	-
QNX Linux	-	-
RTLinux	-	-
Nano-Kernel	Hard Real-Time	1 - 10 μs
ADEOS	-	-
Xenomai	Hard Real-Time	1 - 10 μs

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The suspend latency of RCP scheme support on top of Pentium M plus Pentium 4 scheme perform not surpass 8 μs. The little stop latency creates the structure appropriate intended for approximately every release plus stopped round electrical make. though, it is not fit in favor of motor by SiC support power semiconductor by superior knob freq.

by consider toward the UltraZohm scheme, it be below deliberation toward put in a additional theoretical SW sheet designed for compound information examination.

proposed principle 5: in use method choice

in favor of the Pentium M organization, a number of essential training system intended for apply FOC be able to be originate inside the addendum of [1], which be planned inside C. It be simple toward settle in the system fast designed for a original engine otherwise a original manage technique. through the previous years, additional plus added manage technique be executed resting on a examination worktable support the Pentium M scheme,

since be able to be perceive inside Fig. a agenda organization be reviewtoward evidently here the thought intended for apply dissimilar manage algorithms, such since FOC, DTC, PTC, etc. particularsystem intended for the fundamental PTC way be decorated within azure.

Fig illustrate the plan arrangement intended for the Pentium 4 scheme. It must exist renowned to the plan arrangement intended for Pentium 4 scheme be execute via a master scholar intended for the investigate apply on Technical University of Munich. The immediate algorithms be involuntary within C since Linux kernel component which are activate via an outside disrupt as of FPGA. The Quartus II SW be apply toward plan FPGA in addition to CPLD. by the Pentium 4 structure, antenna fewer technique support saliency [9] in addition to I oversampling [10] be productively execute.

proposed principle 6: useful agenda structure

trial outcome

It focus largely on top of the RCP structure as an alternative of original manage algorithm. so, within regulate toward estimate the presentation, essential MPC way determination exist apply inside a two-stage motor examination worktable support Pentium M structure, a three-stage motor examination worktable support Pentium 4 method [11], plus a two-stage motor examination worktable support UltraZohm arrangement [6].

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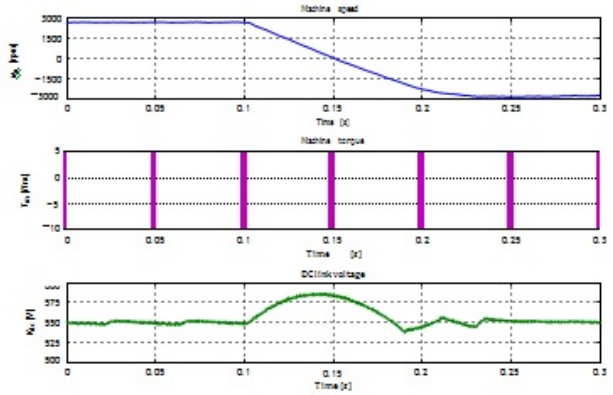

Fig. 8: Speed reversal in the range of whole speed [11]

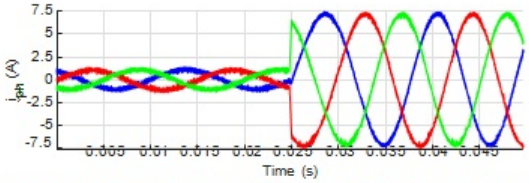

Fig. 9: Three-phase stator currents with reference current step from 1 A to 7 A [6]

TABLE IV: Performance comparison among different test bench.

Control System	Sampling Frequency	Switching Frequency
Pentium M system	16 kHz	3.5 kHz
Pentium 4 system	12 kHz	1.9 kHz
UltraZohm system	100 kHz	23 kHz

two-stage motor plus extent procedure. One engine, determined via a Danfoss VLT FC-302 3.0 kW motor, be employ since consignment engine. The operational engine be determined via a customized SERVOSTAR620 14kVA motor which offer occupied manage of the IGBT entry. The example plus manage freq be put toward be 16 kHz plus DC connection electrical energy be put toward 580 V.

Two-stage motor examination worktable stand Pentium M arrangement

A two-stage motor examination worktable have of a Pentium M scheme, two 2.2 kW accumulator enclose initiation equipment, two Fig. Illustrate a rate setback as of the optimistic insignificant rate +2772 RPM toward the pessimistic insignificant rate RPM by no weight. The recital of engine velocity, torque, I plus change be able to exist perceived. It be evidently to the regulatorhave rejection troubles toward reverse the engine rate.

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A. Three-stage motor experiment worktable support Pentium 4 scheme

A three-stage motor experiment worktable having of the Pentium 4 scheme, one introduction motor plus a self-designed three-stage motor. The example plus manage freq be put to be 12 kHz plus DC connection be motorized 550 V via a 3 kW DC supremacy deliver.

The PTC algorithm is simply complete to three-Stage impartial end compress motors. The fundamental algorithm plus the forecast eqns perform not require toward be misused.

A rapidity turnaround as of the optimistic supposed pace +2772 RPM toward the unhelpful supposed pace RPM by no fill. The presentation of engine rate, torque, I with DC connection electrical energy be able to be observe. It be obviously to the regulator have refusal troubles toward motor the engine pace.

C. Two-stage motor experiment worktable support UltraZohm scheme

A two-stage motor experiment worktable have the UltraZohm scheme, one eternal lure synchronous engine plus a two-stagel motor. The current manage round be congested straight inside FPGA plus employ a straight MPC technique by a example plus organize freq 100 kHz.

The stator I of PMSM by 4 extremity duo consecutively on rate 1200 RPM. The MPC algorithm consecutively in FPGA be able to exist perform each 10 μs, consequential inside a standard knob of 23 kHz. presentation evaluation between the declare experiment worktable be specified. The example plus run freq of UtraZohm stand examination worktable be able to exist sooner than additional scheme. so, it be able to too appropriate manage the motor by the control freq of semiconductor on a elevated stage.

FINALE

The dissimilar RCP scheme intended for manage of PE plus electrical make be offered. It supportive intended for analyzers, who require toward expand the individual RCP scheme otherwise employ a designed authoritative RCP scheme toward execute the difficult algorithms. The Pentium M & Pentium 4 scheme be establish toward exist a practical implement intended for lab test, such the same as fundamental PTC algorithm execution by manage freq positive toward 24 kHz. The UltraZohm scheme be fit designed for manage of complex topologies, difficult plan, plus motor by original extensive posse hole semiconductors, which require quicker manage freq plus additional calculation power. inside the prospect, additional RCP scheme support resting on the latest UltraZohm scheme resolve exist make. Of way, the UltraZohm scheme resolve exist carry on minimized intended for the manage of PE plus electrical make.

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